Preliminary Data Sheet

MAX2980

HomePlug Analog Front End including ADC, DAC, filters, and line driver for power line communications.

The MAX2980 HomePlug Power Line Analog Front End (AFE) integrated circuit is a state-of-the-art CMOS device, which delivers high performance and low cost. This highly integrated design combines the analog-to-digital converter (ADC), digital-to-analog converter (DAC), signal conditioning, and power line driver. The MAX2980 substantially reduces previously required system components, while meeting the HomePlug V1.0 standard. This device interfaces with any companion Digital PHY integrated circuit (IC) to provide a complete HomePlug solution.

The advanced design of the MAX2980 allows operation without external control, enabling simplified connection to a variety of HomePlug Digital PHY ICs. Additional power reduction techniques can be employed through the use of various control signals.

The MAX2980 is specified over the 0ºC to +70ºC commercial temperature range and is offered in a 64-pin LQFP package. can be employed through the use of various control signals.

Applications

High Speed Data over Powerline (SOHO)
Audio/Video Transmission over Powerline
Voice/Modem Transmission over Powerline
Delivering Broadband Access (PLC)
Powerline-to-WiFi Bridge
Powerline-to-DSL Bridge
Powerline-to-Ethernet Bridge
Powerline-to-USB Bridge
Industrial Automation (Monitoring and Control)
Home Automation (Smart Homes)
Security (Cameras)

MAX2980

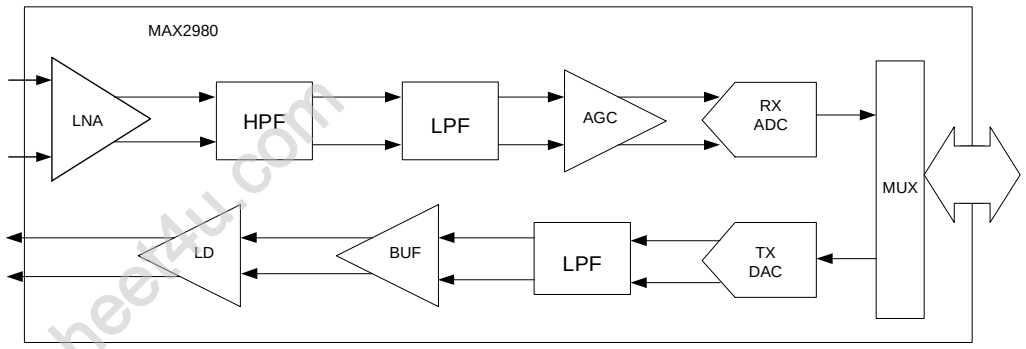
HomePlug Analog Front End

Features:

- Fully Integrated Line Driver and Receiver
- Seamless Interface to Digital PHY ICs
- 10-Bit ADC and DAC with 50 MHz Sampling
- 52dB Adaptive Gain Control
- -139dBm/Hz Input Referred Noise Density
- Transmit Output Spectral Power Density of -52dBm/Hz into 50Ω
- 3.0V to 3.6V I/O
- 270mA in RCV Mode and/or 150mA in XMT Mode at 3.3V
- 64-Pin LQFP Package

PART	TEMP. RANGE	PIN-PACKAGE
	0°C to +70°C	64 LQFP

MAX2980 AFE System Block Diagram



ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD3} = +3.3V, DV_{DD} = V_{REGOUT}, AGND = DGND = SHDN = 0, T_A = 0ºC to 70ºC, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	AV_{DD}, DV_{DD3}			3.0		3.6	V
	DV_{DD}	Because DVDD is connected to Veregout, we can remove this line !!!!!!!!		TBD	2.5	TBD	V
Quiescent Supply Current	I_{DD}	Receive Mode			270		mA
		Transmit Mode	Normal Operation		280		
			Receiver Disabled, /SHRCV\ = high		155		
Shutdown Supply Current					TBD		µA
Regulator Output	V_{REGOUT}	It needs capacitors probably!			2.5		V
Bandgap Voltage					1.29		V
Output Voltage High	V_{OH}			2.4			V
Output Voltage Low	V_{OL}					0.4	V
LOGIC INPUT CHARACTERISTICS							
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage current High	I_{IH}	V_{IH} = VDD				+10	µA
Input Leakage current Low	I_{IL}	V_{IL} = 0		-10			µA
INPUT AND OUTPUT CLAMPS (TBD)							
Input Clamp Voltage		Negative Rail, I_{CL} = -18mA				-0.8	V
		Positive Rail, I_{CL} = 18mA				**+0.8**	
Output Clamp Voltage		Negative Rail, I_{CL} = -18mA				–0.8	V
		Positive Rail, I_{CL} = 18mA				+0.8	
ANALOG-to-DIGITAL CONVERTER (ADC) CHARACTERISTICS							
Resolution	N				**10**		Bits
Integral Nonlinearity	INL					2	LSB
Differential Nonlinearity	DNL					1	LSB
Two-Tone Third-Order Distortion	IM3	2-tones at 17MHz and 18MHz, $1V_{PP}$, Differential.		55			dB
Effective Number of Bits	ENOB			9.5			Bits
DIGITAL-to-ANALOG CONVERTER (DAC) CHARACTERISTICS							
Resolution	N				10		Bits
Integral Nonlinearity	INL					1.5	LSB
Differential Nonlinearity	DNL					0.5	LSB
Two-Tone Third-Order Distortion	IM3	2-tones at 17MHz and 18MHz, $1V_{PP}$, Differential.		42			dB
Effective Number of Bits	ENOB			9			Bits
RECEIVER CHARACTERISTICS							
Common-Mode Voltage		Pins PLIP/PLIN			1.62		V
Input Noise						-139	dBm/Hz
Input Impedance	Z_{IN}	Between pins PLIP and PLIN			170		Ω
Two-Tone Third-Order Distortion	IM3	2-tones at 17MHz and 18MHz, $1V_{PP}$, Differential.		50			dB

Gain Control Range	AGC			-9	44	dB
Frequency Accuracy		**TBD**			TBD	TBD
TRANSMITTER CHARACTERISTICS						
Common-Mode Voltage		Pins PLOP/PLON		1.59		V
Output Impedance	Z_{OUT}				2.5	Ω
Short Circuit Current	I_{SC}				300	mA
Output Power Spectral Density	PSD	R_L = 50Ω,	Pre driver gain = 3dB	-54.55		dBm/Hz
			Pre driver gain = 1dB	-55.9		
			Pre driver gain = -6dB	-63.13		
Two-Tone Third-Order Distortion	IM3	2-tones at 17MHz and 18MHz, $1V_{PP}$, Differential.		42		dB
Output Drive				10		Ω

TIMING CHARACTERISITICS (Figure 1)

(AV_{DD} = DV_{DD3} = +3.3V, DV_{DD} = V_{REGOUT}, AGND = DGND = SHDN = 0, T_A = 0ºC to +70ºC, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

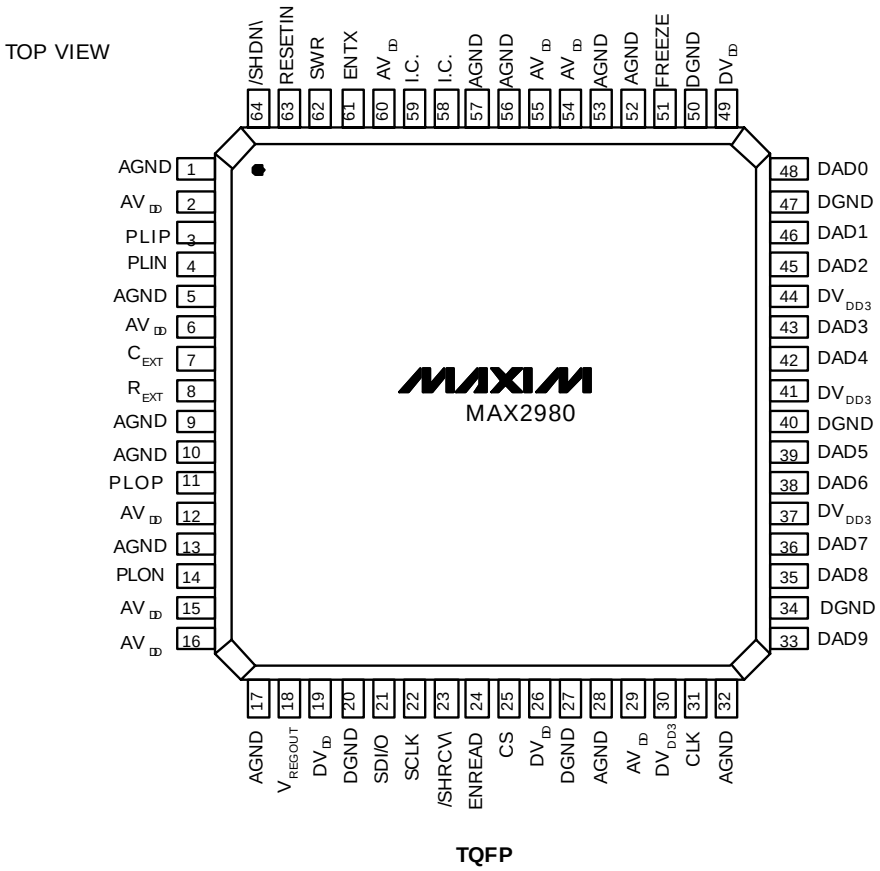
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Frequency				50		MHz
CLK Tolerance			-25		+25	ppm
CLK Fall to ADC Data Output Valid Time	t_{ADCO}	Note 2	-3	2	7	ns
CLK Fall to DAC Data Latch Time	t_{DACI}	Note 2	-2	3	8	ns

MAX2980 Pin Description

PIN	NAME	FUNCTION
1, 5, 9, 10, 13, 17, 28, 32, 52, 53,56,57	AGND	Analog Ground
2, 6, 12, 15, 16, 29, 54, 55, 60	AV_{DD}	Analog Power-Supply Voltage. AV_{DD} supply range is 3.0V to 3.6V. Bypass AV_{DD} with a TBDµF capacitor to AGND.
3	PLIP	AC Power Line Positive Input
4	PLIN	AC Power Line Negative Input
7	C_{EXT}	External Capacitor Connection. Connect a 10nF Capacitor from CSG to AGND.
8	R_{EXT}	External Resistor Connection. Connect a 25kΩ resistor from EXT to AGND.
11	PLOP	AC Power Line Positive Output
14	PLON	AC Power Line Negative Output
18	V_{REGOUT}	Voltage Regulator Output. Connect V_{REGOUT} to DV_{DD} for normal operation.
19, 26, 49	DV_{DD}	Digital 2.5V Voltage Input. Connect to V_{REGOUT} for normal operation.
20, 27, 34, 40, 47, 50	DGND	Digital Ground
21	SDI/O	Serial Data Input and Output
22	SCLK	Serial Clock Input
23	/SHRCV\	Receiver Shut-Down Control. Drive /SHRCV\ high to power down receiver. Drive low for normal operation.

24	ENREAD	Read Mode Enable Control. Drive ENREADhigh to place the DAD[9:0] bi-directional buffers in read mode. Data are transferred from the Digital PHY to the AFE DAC. ENREAD signal frames the transmission.
25	CS	Active-High Carrier Select Input. Drive CS high to initiate the internal timer.
30, 37, 41, 44	DV_{DD3}	Digital Power-Supply Voltage. DV_{DD3} supply range is 3.0V to 3.6V. Bypass DV_{DD3} to DGND with a TBDµF capacitor as close to pin as possible.
31	CLK	50MHz System Clock Input
33	DAD9	DAC/ADC Input/Output MSB Data Bit . Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
35	DAD8	DAC/ADC Input/Output Data Bit 8. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
36	DAD7	DAC/ADC Input/Output Data Bit 7. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
38	DAD6	DAC/ADC Input/Output Data Bit 6. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
39	DAD5	DAC/ADC Input/Output Data Bit 5. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
42	DAD4	DAC/ADC Input/Output Data Bit 4. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
43	DAD3	DAC/ADC Input/Output Data Bit 3. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
45	DAD2	DAC/ADC Input/Output Data Bit 2. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
46	DAD1	DAC/ADC Input/Output Data Bit 1. Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
48	DAD0	DAC/ADC Input/Output LSB Data Bit . Input/Output of 10-bit, 50MHz bi-directional digital-to-analog and analog-to-digital converter. Data is in binary format.
51	FREEZE	Active-High Freeze Mode Enable. Drive FREEZE high to place the AGC adaptation in freeze mode. Drive FREEZE low, if the the signal is not available for the companion baseband chip.
58, 59	I.C.	Internally Connected. Leave these pins floating.
61	ENTX	Active-High Transmit Enable. Drive ENTX high to enable the transmitter. Drive ENTX low to place transmitter in tri-state.
62	SWR	Active-High Register Write Enable. Drive SWR high to place the registers in write mode.
63	/RESETIN\	Active-Low Reset Input. Drive /RESETIN\ low to place the MAX2980 into reset mode. Set CLK in free-running mode during a reset. The minimum reset pulse width is 100ns.
64	SHDN	Active-High Shutdown Input. Drive SHDN high to place the MAX2980 into shutdown mode. Drive low for normal operation.

MAX2980 Pin Diagram



TQFP

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +3.9V
$DV_{DD3\_}$ to DGND ..... -0.3V to +3.9V
DV_{DD} to DGND.....-0.3V to +**TBD**V
AGND to DGND.....-0.3V to +0.3V
All Other Pins.....-0.3V to (V_{DD} + 0.3V)
Current Into Any Pin.....±100mA
Short-Circuit Duration (V_{REGOUT} to AGND).....Continuous **<<??>>**
Continuous Power Dissipation (T_A = +70°C)
64-Pin LQFP (derate **TBD**mW/°C above +70°C).....**TBD**mW
<<Part is not listed in Parts File, so Power Dissipation info is TBD>>
Operating Temperature Range .....0°C to +70°C
Junction Temperature.....+150ºC
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Detailed Description

The MAX2980 HomePlug Power Line Analog Front End (AFE) integrated circuit is a state-of-the-art CMOS device, which delivers high performance and low cost. This highly integrated design combines the analog-to-digital converter (ADC), digital-to-analog converter (DAC), signal conditioning, and power line driver as shown in the block diagram of Figure 1. The MAX2980 substantially reduces previously required system components, while meeting the HomePlug V1.0 standard. This device interfaces with any companion Digital PHY IC to provide a complete HomePlug solution.

The advanced design of the MAX2980 allows operation without external control, enabling simplified connection to a variety of HomePlug Digital PHY chips. Additional power reduction techniques can be employed through the use of various control signals.

Receive Channel

The receiver analog front end consists of a low-noise amplifier (LNA), a high-pass filter (HPF), a low-pass filter (LPF), and an automatic gain control circuit (AGC). An analog-to-digital converter (ADC) block samples the AGC output. The ADC communicates to the Digital PHY Chip through a MUX block.

The LNA reduces the receive channel input-referred noise by providing some signal gain to the AFE input.

The filter blocks remove unwanted noise, and provide the anti-aliasing required by the ADC for accurate sampling. The combination of a low-pass filter and a high pass filter keeps the bandwidth in the desired range of 4.49MHz to 20.7MHz, as required in the Homeplug specification.

The automatic gain control (AGC) scales the signal for conversion from analog to digital. The scaling maintains the optimum signal level at the ADC input, and keeps the AGC amplifiers out of saturation.

The 50MHz, 10-bit ADC samples the analog signal and converts it to a 10-bit digital stream. The block fully integrates reference voltages and biasing for the input differential signal.

Transmit Channel

The transmit channel consists of a 10-bit digital-to-analog converter (DAC), a low-pass filter, and a transmitter buffer and line driver. The DAC receives the data stream from the Digital PHY IC through the MUX block.

The 50MHz, 10-bit DAC provides the complimentary function to the receive channel. The DAC converts the 10-bit digital stream to an analog voltage at a 50MHz rate.

The low-pass filter removes spurs and harmonics adjacent to the desired passband to help reduce the out of band transmitted frequencies and energy from the DAC output. The filter allows the MAX2980 to meet the Homeplug Alliance Specification.

The transmit buffer and line driver blocks allow the output level of the low-pass filter to obtain a level necessary to connect directly to the powerline medium, without the use of external amplifiers and buffers. The output level is adjustable between $0.5V_{RMS}$ and $0.75V_{RMS}$. The line driver can drive resistive loads as low as 10Ω.

There are some repeted sentence, remove them all!

Digital Interface

The digital interface is composed of some control signals and a 10-bit bi-directional data bus for the DAC and ADC. The control signals include a reset line, a transmit request, an I/O detection request, and a shutdown control.

Control Signals

Transmit Enable (ENTX)

The ENTXline is used to enable the transmitter of the MAX2980 AFE circuit. With ENTXand ENREADdriven high, data sent to the DAC through DAD[9:0] is conditioned and delivered onto the power line.

Read Enable (ENREAD)

The ENREAD line sets the direction of the data bus DAD[9:0]. With ENREAD high, data is sent from the Digital PHY to the DAC in the MAX2980 AFE. A low on ENREAD sends data from the ADC to the Digital PHY.

Receiver Powerdown (/SHRCV\)

The /SHRCV\ line provides receiver shutdown control. A logic high on /SHRCV\ powers down the receiver section of the MAX2980 whenever the device is transmitting. The MAX2980 also features a transmit power savings mode which reduces supply current from **TBD**mA to **TBD**mA. To enter the transmit power savings mode, drive /SHRCV\ high **TBD**µs prior to the end of transmission. Connect /SHRCV\ to ENTXand ENREADfor normal operation.

Digital-to-Analog and Analog-to-Digital Converter Input/Output. (DAD[9:0])

DAD[9:0] is the 10-bit bi-directional bus connecting the Digital PHY to the MAX2980 AFE DAC and ADC. The bus direction is controlled by ENREAD, as described in the *Read Enable* section.

AGC Control Signal(CS)

The CS signal controls the AGC circuit of the receive path in the MAX2980. A logic low on CS sets the gain circuit on the input signal to continuously adapt for maximum sensitivity. A valid preamble detected by the Digital PHY raises CS to high. While CS is high, the AGC continues to adapt for an additional short duration, then it locks the currently adapted level on the incoming signal. The Digital PHY holds CS high while receiving a transmission, and then lowers CS for continuous adaptation for maximum sensitivity of other incoming signals.

AGC Freeze Mode (FREEZE)

Use the FREEZE signal to lock the AGC gain. Note if CS or FREEZE is not used, the maximum loss in SNR is 1dB due to modulation effects generated by the AGC circuit on some selective channels.

Clock (CLK)

The CLK signal provides all timing for the MAX2980 AFE. Apply a 50MHz clock to this input. See timing diagram of figure 1 for more information.

Reset Input (/RESETIN\)

The /RESETIN\ signal provides reset control for the MAX2980. To perform a reset, set CLK in free running mode and drive /RESETIN\ low for a minimum of 100ns. Always perform a reset at power-up.

Shutdown Control (SHDN)

The MAX2980 features a low-power, shutdown mode that is activated by SHDN. Drive SHDN high to place the MAX2980 in shutdown mode. In shutdown, the MAX2980 consumes only **TBD**µA.

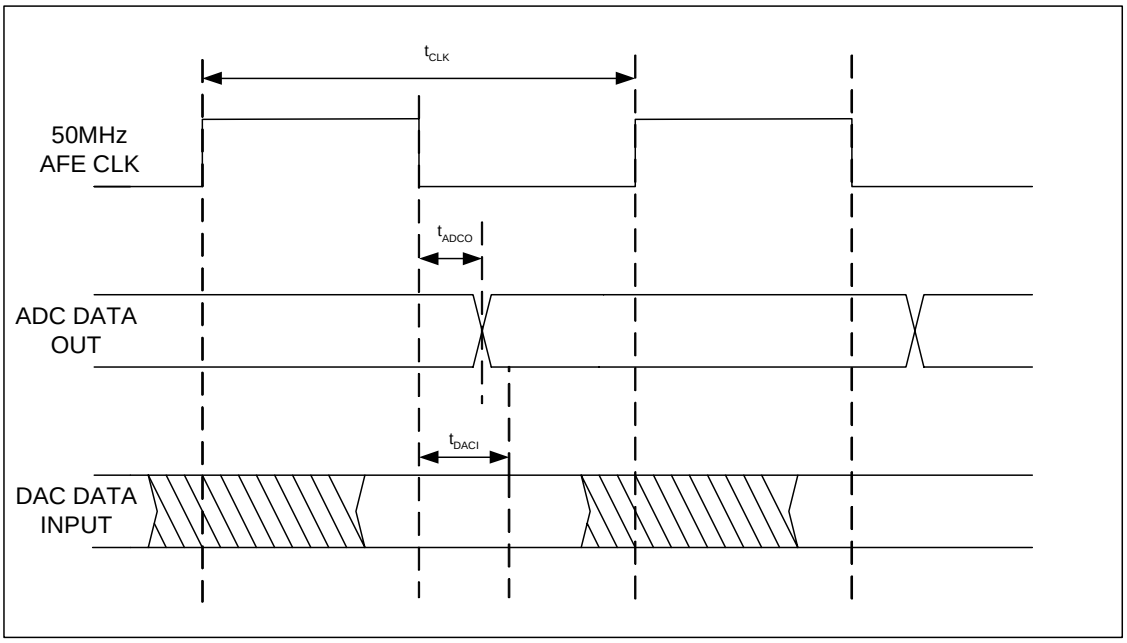


Figure 1. ADC and DAC Timing Diagram

MAX2980 Control Registers
MAX2980 Serial Interface

The 3 wire serial interface controls the MAX2980 AFE operation mode. The **SCLK** is the serial clock line for register programming. The **SDI/O** is I/O serial data input and output for register writing or reading. The **SWR** signal controls WRITE/READ mode of the serial interface.
If **SWR** is HIGH the serial interface is in WRITE mode and new value can be written into AFE registers. Following **SWR** low-to-high transition, data are shifted synchronously to AFE (LSB first) register on the falling edge of the serial clock (**SCLK**) as illustrated in Figure 2. Note that one extra clock **(WR_CLK**) is required to write the content of holding buffer to the appropriate register bank.
If **SWR** is LOW the serial interface is in READ mode and value of the current AFE register can be read. The Read operation to specific register must be followed right after writing to the same AFE register. Following **SWR** high-to-low transition, data are shifted synchronously to AFE (LSB first) register on the falling edge of the serial clock (**SCLK)** as illustrated in Figure 3.

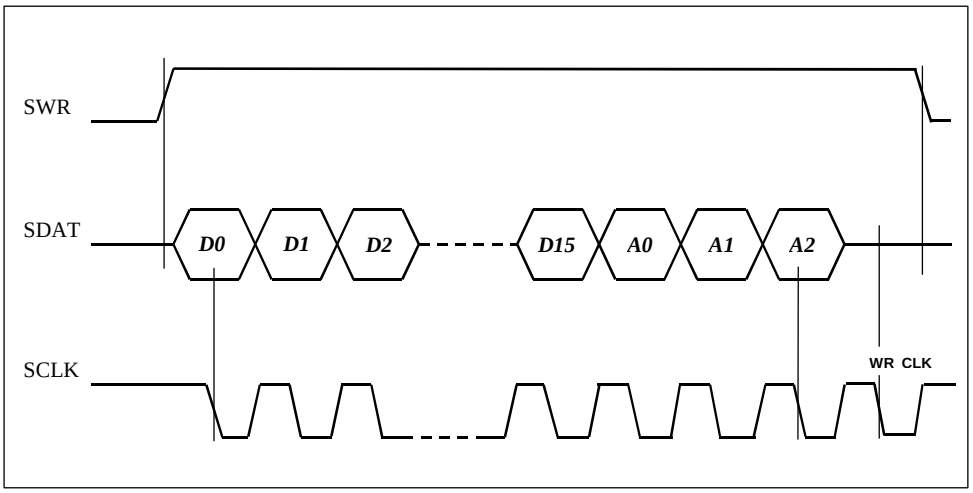


Figure 2. Writing AFE register timing diagram.

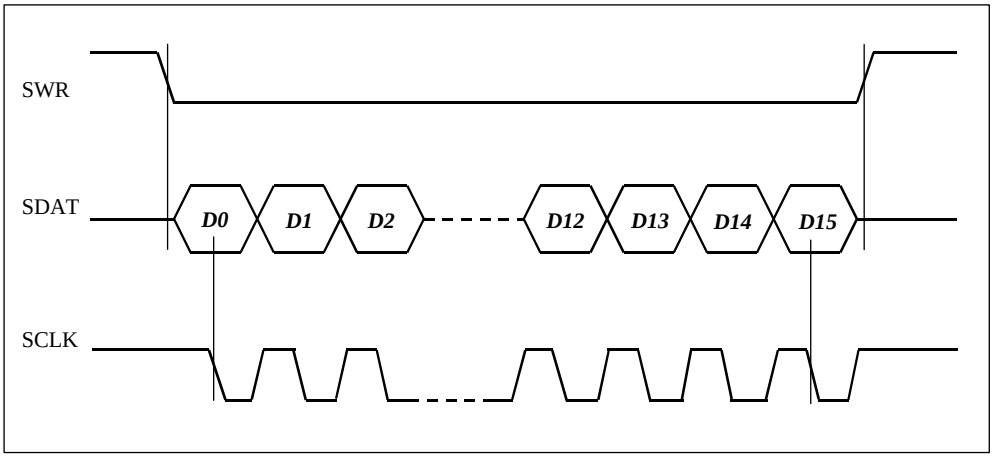


Figure 3. Reading AFE register timing diagram.

The MAX2980 has a set of six READ/WRITE registers, bits A2-A0 are the AFE register address bits.

Table 1: AFE registers address:

Register	A2	A1	A0
R1 (R/W)	0	0	0
R2 (R/W)	0	0	1
R3 (R/W)	0	1	0
R4 (R/W)	0	1	1
R5 (R/W)	1	0	0
R6 (R/W)	1	0	1

MAX2980 AFE Register Maps

Table2. Register R1 Map

Register Bit No.	Default	Comment
R1B0	LOW	Active HIGH, power downs Receiver when in transmit mode. Based on /SHRCV\ signal going HIGH, (Enable SMT1 mode)
R1B1	HIGH	Active HIGH, power down transmitter when in receive mode, based on XMT signal going High, (Enables SMT2 mode)
R1B2	LOW	Active HIGH, power down DAC when in Receive mode, based on XMT signal going HIGH (SMTDA mode)
R1B3	LOW	Active HIGH, power down entire chip
R1B4	LOW	For test purposes
R1B5	LOW	For test purposes
R1B6	LOW	For test purposes
R1B7	LOW	For test purposes
R1B8	LOW	For test purposes
R1B9	LOW	For test purposes
R1B10	LOW	For test purposes
R1B11	LOW	For test purposes
R1B12	LOW	For test purposes
R1B13	LOW	For test purposes
R1B14	LOW	For test purposes
R1B15	LOW	For test purposes

Note: From Bit 4 to Bit 15 control power down on various blocks.

Table 3. Register R2 Map

Register Bit No.	Default	Comment
R2B0	LOW	For test purposes
R2B1	LOW	For test purposes
R2B2	LOW	For test purposes
R2B3	HIGH	Active HIGH, bypass the HPF
R2B4	LOW	For test purposes
R2B5	LOW	For test purposes
R2B6	LOW	For test purposes
R2B7	LOW	For test purposes
R2B8	LOW	For test purposes
R2B9	LOW	For test purposes
R2B10	LOW	For test purposes
R2B11	LOW	For test purposes
R2B12	LOW	For test purposes
R2B13	LOW	For test purposes
R2B14	LOW	For test purposes
R2B15	LOW	Active HIGH, bypass the receive LPF

Note: From Bit 0 to Bit 2 and Bit 4 to B14 must be set to LOW to disable connection to the Test Bus.

Table 4. Register R3 Map

Register Bit No.	Default	Comment
R3B0	LOW	Set OFFSET DAC parameters. For test purposes.
R3B1	LOW	
R3B2	LOW	These set the pre-driver gain as follows setting 000 to 111: 3dB, 2dB, 1dB, 0dB, -1dB, -2dB, -3dB, -6dB R3B2 is the LSB
R3B3	LOW	
R3B4	LOW	
R3B5	LOW	Override process tune setting. For test purposes.
R3B6	LOW	
R3B7	LOW	
R3B8	LOW	
R3B9	LOW	
R3B10	LOW	
R3B11	HIGH	Active HIGH, place process tune in continuous mode, otherwise active only during RESET
R3B [15:12]	0111	Set to control the gain scaling in the DAC. For test purposes

Table 5. Register R4 Map

Register Bit No.	Default	Comment
R4B0	LOW	Active HIGH, allow VADAPT continuous offset cancellation, otherwise offset cancellation stops on FREEZE = HIGH
R4B1	HIGH	Active HIGH, allow HIGH to LOW transition of CS to control adaptation reset
R4B2	HIGH	Active HIGH, enable 8us delay of offset cancellation FREEZE after FREEZE is active, otherwise delay = 0us.
R4B3	HIGH	Active HIGH, enable freeze of VGA/OFFSET adaptation 20us (or 30us if en_30u is selected) after LOW to HIGH transition of CS 'OR' on FREEZE input. When R4B3 is LOW, freeze will only take place on FREEZE HIGH.
R4B4	LOW	Active HIGH, enable adaptation energy detect to clear adaptation after loss of signal. When low this circuits disabled and CLR will be based on HIGH to LOW transition of CS.
R4B5	LOW	For test purposes.
R4B [10:6]	01011	Load adaptation RMS target reference level M as follows: '00000' to '11111'. N = M+6 and level in RMS = sqrt (32N)/128 for N <= 32 and Level RMS = sqrt(128(N-24))/128 for N > 32. Default is N=32 or 250mVrms {ref_load}
R4B11	HIGH	For test purposes
R4B12	HIGH	For test purposes
R4B13	HIGH	These two set the peak detector reference level as follows: '00' 0.15V, '11' 0.10V, '10' 0.18V, '01' 0.20V where R4B13 is the LSB. [For V1: "00" 0.2V, "11" 0.15V].
R4B14	HIGH	
R4B15	LOW	For test purposes

Table 6. Register R5 Map

Register Bit No.	Default	Comment
R5B [6:0]	LOW	Set to control manually VGA & offset cancellation circuits. LOW for automatic adaptation.
R5B [12:7]	LOW	
R5B13	LOW	
R5B14	LOW	
R5B15	LOW	

Table 7. Register R6 Map

Register Bit No.	Default	Comment
R6B0	LOW	For test purposes. ADC test only.
R6B [2:1]	00	For test purposes
R6B3	LOW	For test purposes
R6B4	LOW	Active HIGH, allow BYPASS of transmit LPF
R6B [6:5]	00	Used to set the parameter of VGA and DC offset cancellation algorithm. For test purposes.
R6B7	LOW	
R6B8	LOW	
R6B9	LOW	
R6B [11:10]	10	
R6B [13:12]	00	
R6B14	HIGH	
R6B15	HIGH	

Applications Information

Interfacing to Digital PHY Circuit

The MAX2980 interfaces to a Homeplug 1.0 Digital PHY IC using a bi-directional bus to pass the digital data to and from the DAC and ADC. Handshake lines help accomplish the data transfer and operation of the MAX2980. The application circuit diagram of Figure 4 shows the connection of the MAX2980 to the digital PHY and the powerline.

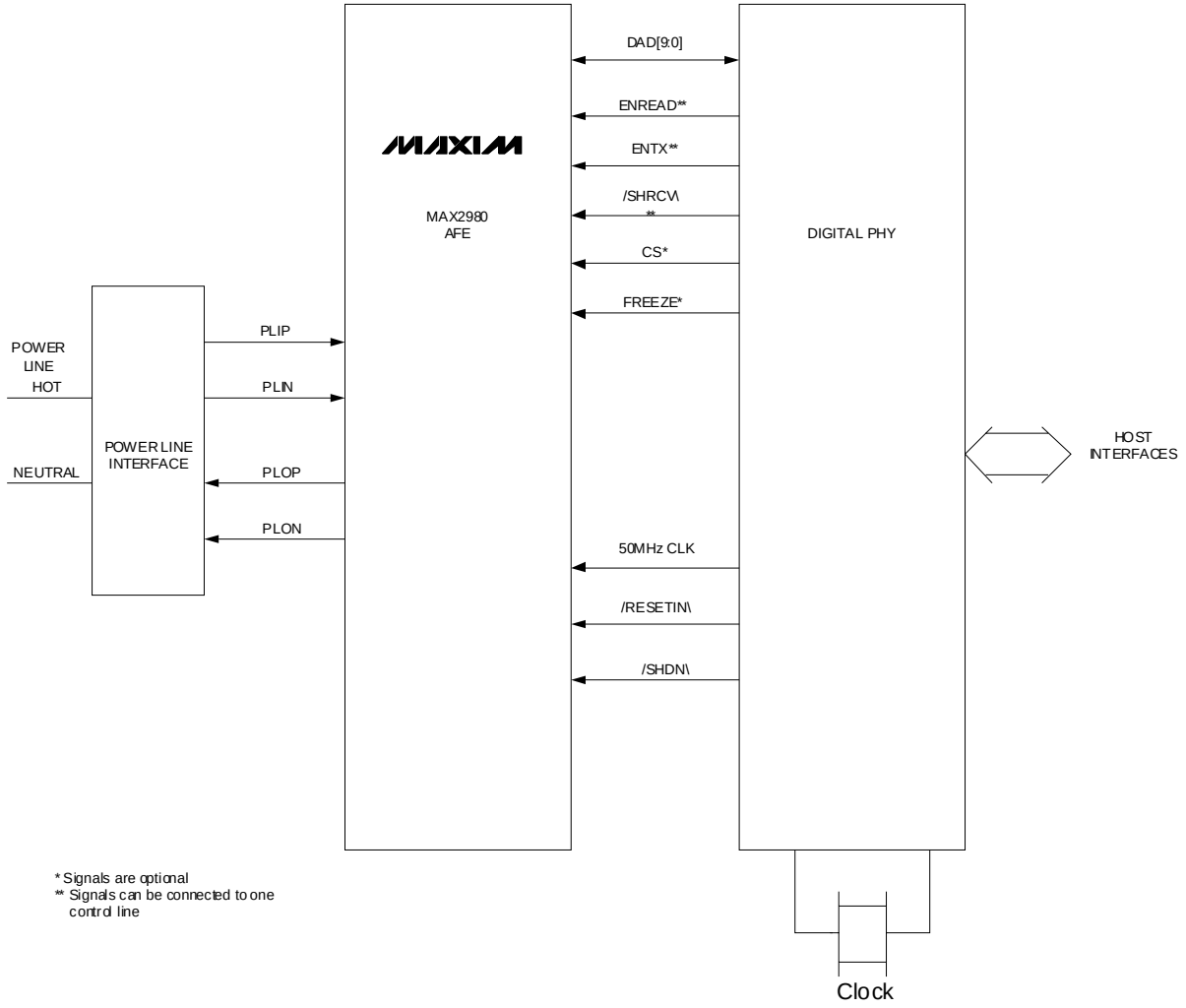


Figure 4. Interfacing the MAX2980 to a Digital PHY Circuit and Power Line.

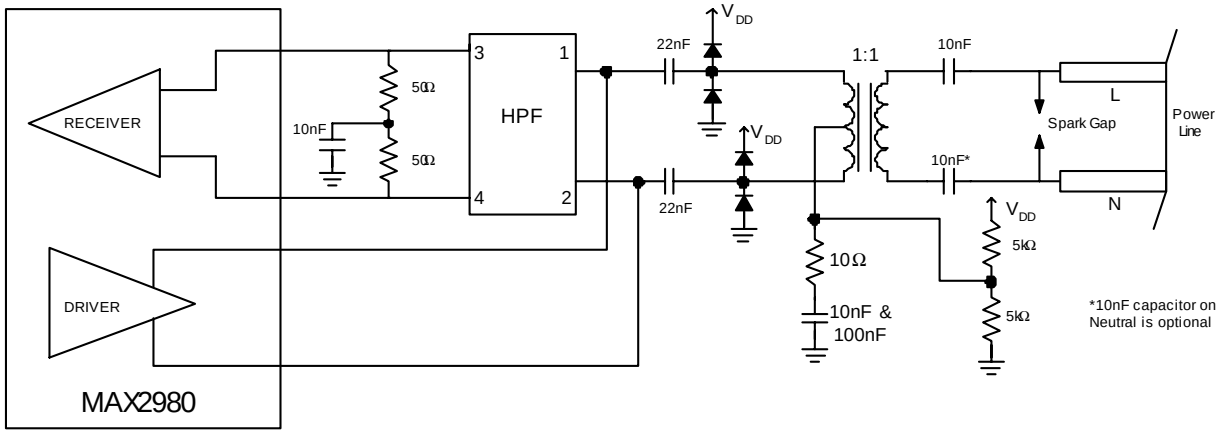
Layout Considerations

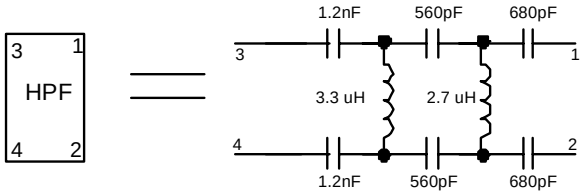
A properly designed PC board is an essential part of any high-speed circuit. Use controlled impedance lines on all frequency inputs and outputs. Use low inductance connections to ground on all ground pins and wherever the components are connected to ground. Place decoupling capacitors close to all VCC connections. For proper operation, connect the metal exposed paddle at the back of the IC to PCB ground plane with multiple vias.

Chip Information

Process: CMOS
Transistor Count: **TBD**

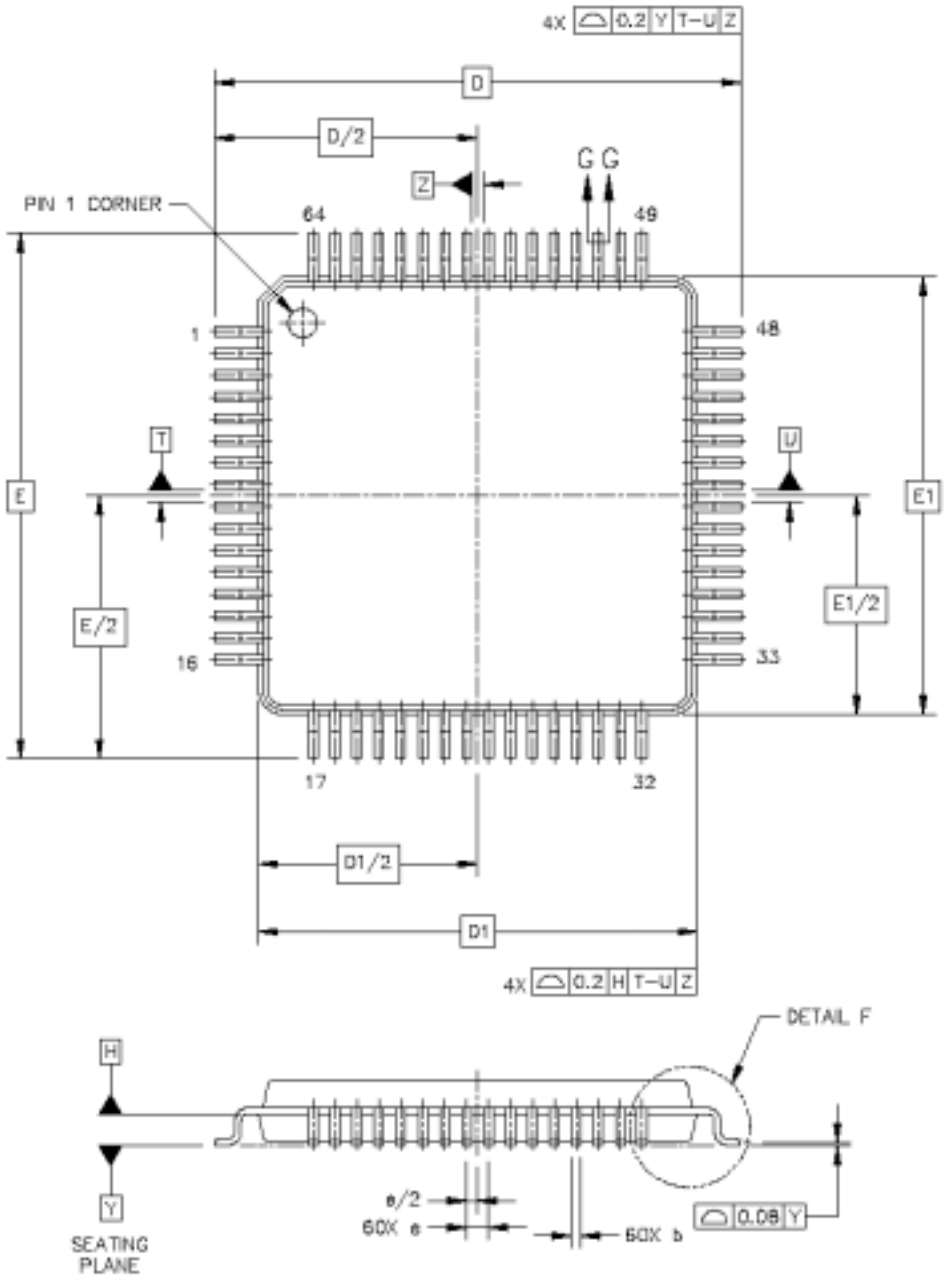
Typical Application





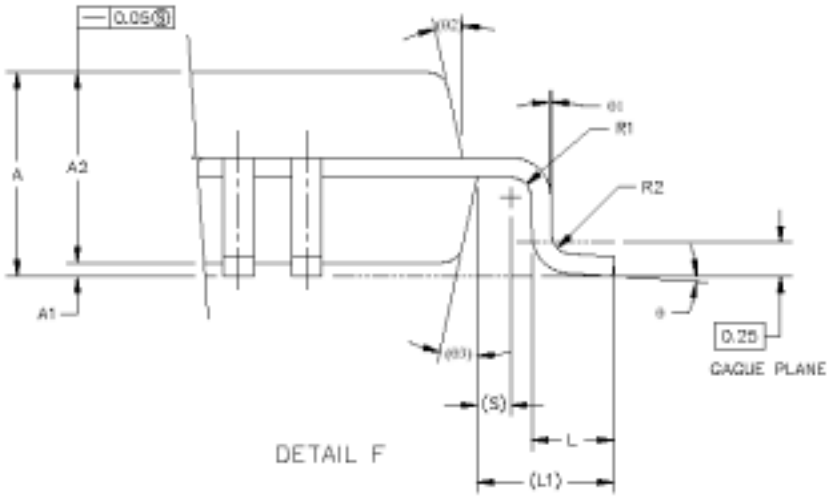
Package Information

ASE (Chung-Li), Inc.	PACKAGE OUTLINE	DWG NO.	98A0064QP002
		ISSUE	O
		DATE	17AUG2000

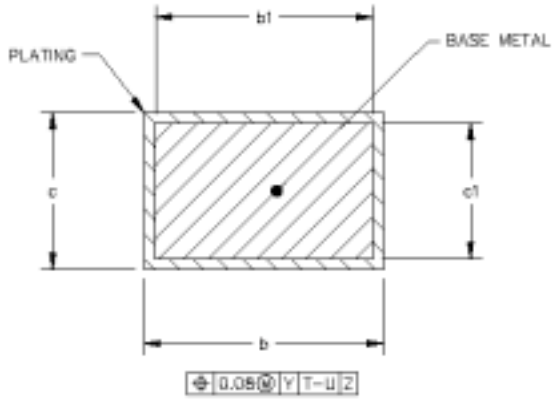


TITLE: LQFP 64 LD 10X10X1.4 PKG 0.5 PITCH POD	COMPANY	ASECL
	SHEET	1 OF 3

ASE (Chung-Li), Inc.	PACKAGE OUTLINE	DWG NO.	98A0064QP002
		ISSUE	O
		DATE	17AUG2000



DETAIL F



SECTION G-G

TITLE: LQFP 64 LD 10X10X1.4 PKG 0.5 PITCH POD	COMPANY	ASECL
	SHEET	2 OF 3

Parameter	Description	Value
Package Material	Sumitomo EME 6600CS (low stress compound)	
Lead Surface Material	Solder Plate: 63% Sn, 37% Pb	
Lead Base Material	Copper	
θ_{JC}	Junction to Case Thermal Resistance	7 °C/W
θ_{JA}	Junction to Ambient Thermal Resistance, 0m/s air flow, no heat sink	37 °C/W

ASE (Chung-Li), Inc.	PACKAGE OUTLINE	DWG NO.	98A0064QP002
		ISSUE	O
		DATE	17AUG2000

NOTES:

1. DIMENSOIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

DIM	MIN	MAX	DIM	MIN	MAX	DIM	MIN	MAX
A	---	1.6	L1	1 REF				
A1	0.05	0.15	R1	0.1	0.2			
A2	1.35	1.45	R2	0.1	0.2			
b	0.17	0.27	S	0.2 REF				
b1	0.17	0.23	θ	0°	7°			
c	0.09	0.2	θ1	0°	---			
c1	0.09	0.16	θ2	12° REF				
D	12 BSC		θ3	12° REF				
D1	10 BSC							
e	0.5 BSC							
E	12 BSC							
E1	10 BSC							
L	0.45	0.75						

TITLE: LQFP 64LD 10X10X1.4 PKG 0.5 PITCH POD	COMPANY	ASECL
	SHEET	3 OF 3